S.N. 10/505,216 Docket No.: 1374.43896X00 Page 9

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated August 8, 2005. by the present amendment, the claims have been amended to clarify the invention.

Reconsideration and removal of the 35 USC §102(b) rejection of claims 1-15 as being anticipated by Jung (USP 6,034,884) is respectfully requested. With regard to this, each of the independent claims 1, 10 and 12 has been amended to clearly define the structure of the present invention of forming a nonvolatile memory and a central processing circuit on one semiconductor substrate (as shown, for example, in Fig. 2 with the CPU 2 and a nonvolatile memory, such as the ROM 4, being formed on one semiconductor substrate 1). This is particularly described on page 14, line 12 et seq. of the Substitute Specification with the statement:

"The semiconductor integrated circuit 1 is obtained by forming the following over one semiconductor chip by, for example, a publicly known CMOS integrated circuit fabrication technique; a central processing unit (CPU) 2, RAM 3, ROM 4, a bus controller (BSC) 5 and a peripheral circuit 6."

As such, from the outset, the amended independent claims 1, 10 and 12 are clearly not anticipated by the Jung reference since this reference fails to teach a central processing circuit and a nonvolatile memory being structured on one semiconductor substrate.

In addition, the claims have been amended to further clarify the structure regarding the nonvolatile memory and the central processing circuit to even further distinguish over the Jung reference.

S.N. 10/505,216 Docket No.: 1374.43896X00 Page 10

For example, independent claim 1 has been amended to define that the nonvolatile memory is capable of storing a program and/or data together with defining that the central processing circuit, also formed on the one semiconductor substrate, is capable of fetching a program from the nonvolatile memory. This corresponds to the discussion found, for example, on page 14, lines 17 et seq. Independent claim 10 specifically defines a structure for the construction of the memory cell utilizing a pair of MOS transistors having connections similar to those discussed in regard to Fig. 1. Page 16, line 12 et seq., of the Specification describes Fig. 1 noting that it can be a part of the ROM 4 shown in Fig. 2 (noting, incidentally, that reference to specific figures such as Figs. 1 and 2 is solely for purpose of example). As shown in Fig. 1, and as discussed on page 16, line 15 et seq.:

"Each memory cell 20 comprises a first MOS transistor M1 and a second MOS transistor M2, whose gate electrodes are connected with a corresponding word line in common. The drain electrodes of both the MOS transistors M1 and M2 are joined with the complementary bit lines b1 and b1b. The source electrode of either MOS transistor M1 or M2 is connected with a common source line cs, and the source electrode of the other MOS transistor is floated."

Independent claim 12 defines the features noted above with regard to both independent claims 1 and 10. As such, it is respectfully submitted that each of these independent claims clearly define over the structure of Jung which simply teaches a nonvolatile DRAM having complementary bit lines and memory cells including two transistors, but completely fails to teach or suggest the claimed data processing circuit with the above noted structure including a central processing circuit and a nonvolatile memory structured on one semiconductor substrate.

S.N. 10/505,216 Docket No.: 1374.43896X00 Page 11

With regard to the present rejection, it is noted that this rejection is set forth as an anticipation rejection under 35 USC §102. As noted in the decision *in Re Robertson, 49 USPQ 2d 1949 (Fed. Cir. 1999)*, a rejection under 35 USC §102 for anticipation requires that each and every element as set forth in the claim is found, either expressly or inherently described in the single prior art reference. With regard to this, it is noted that nothing in the Jung reference teaches or suggests the claimed data processing circuit with the central processing circuit and the nonvolatile memory structured on one semiconductor substrate, particularly with the claimed features for the central processing circuit and the nonvolatile memory. Therefore, reconsideration and removal of the 35 USC §102 anticipation rejection is respectfully requested.

Incidentally, it is noted that, although a 35 USC §103 obviousness rejection has not been made, clearly the amended claims of the present application are not obvious over Jung either. With regard to this, the independent claims 1, 10 and 12 each clearly set forth structure which is not only not taught by Jung, but is also not suggested by Jung. As such, it is respectfully submitted that there is no motivation whatsoever for modifying Jung to arrive at the claimed invention as set forth in the amended independent claims 1, 10 and 12 and their respective dependent claims. Therefore, allowance of these claims is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

S.N. 10/505,216 Docket No.: 1374.43896X00

Page 12

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Kindly charge any shortage in the fees or credit any overpayment of fees in connection with the filing of this paper, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 1374.43896X00).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

Gregory E. Montone Reg. No. 28,141

GEM/dks N:\1374\43896X00\AMD\CK3092.DOC

1300 North Seventeenth Street, Suite 1800

Arlington, Virginia 22209 Telephone: (703) 312-6600 Facsimile: (703) 312-6666